QUARTERLY REPORT NO. 13
FOR
ANALOG-TO-DIGITAL CONVERTER
CONTRACT NO. N00014-87-C-0314
1 April 1991—30 June 1991

ARPA Order Number:	7356
Program Code Number:	7220
Amount of Contract:	$3,152,507
Name of Contractor:	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655936, M.S. 105 Dallas, Texas 75265
Effective Date of Contract:	30 March 1987
Contract Expiration Date:	29 February 1992
Contract Number:	N00014-87-C-0314
Program Manager:	W.R. Wisseman (214) 995-2451
Principal Investigator:	Frank Morris (214) 995-6392
Short Title of Work:	GaAs A-to-D Converter
Contract Period Covered by Report:	1 April 1991—30 June 1991

8 July 1991

Approved for Public Release; distribution unlimited

The views and conclusions contained in this document are those of the authors and should not be interpreted as necessarily representing the official policy, either expressed or implied, of the Defense Advanced Research Projects Agency or the United States Government.

QUARTERLY REPORT NO. 13
FOR
ANALOG-TO-DIGITAL CONVERTER
Contract No. N00014-87-C-0314
1 April 1991 – 30 June 1991

I. SUMMARY

A. Brief Program Definition

This is a research and development program to design and fabricate both a GaAs high-sampling-rate converter (ADC) and a high-resolution GaAs ADC.

B. ADC Program Overview

A final p-channel JFET lot is being completed in the GaAs pilot line to establish the correct threshold implant dosage. In-process tests suggest that these PJFETs will meet the required gate-drain breakdown voltage, as well as demonstrate the correct values for saturation currents. The 12-bit ADC mask set is scheduled for release for pilot-line fabrication by mid August.

II. PROGRESS REPORT

A. Process Development

The first PJFET lot fabricated in the GaAs Pilot Line resulted in breakdown voltages less than that required for successful operation of the 12-bit ADC. To solve this problem, a second lot of material was started in which the HBT n-epi collector layer thickness was increased to support a higher breakdown voltage for the PJFETs, which are fabricated in this layer. In addition, a beryllium channel implant matrix was run on this same material to determine correct I_{dss} channel currents. In-process probing after processing the contact metal suggests that the epi changes were successful in solving the low breakdown problem, with typical breakdown voltages exceeding 12 V. The channel implant matrix also appears to have established the desired currents. The lot will complete processing during early July and will be fully characterized shortly thereafter.

B. Circuit Design/Testing

We continue to make progress in the design and layout capture of the 12-bit ADC. The 12-bit ADC circuitry has been partitioned between two ICs to maximize yield and improve testability (Figure 1). The primary IC contains core 12-bit ADC circuitry including sample-and-hold (S/H), 5-bit quantizer, gain-switched residue amplifier, error correction, and TTL driver circuitry. The secondary IC generates internal ADC timing and control signals from a single external TTL clock strobe.

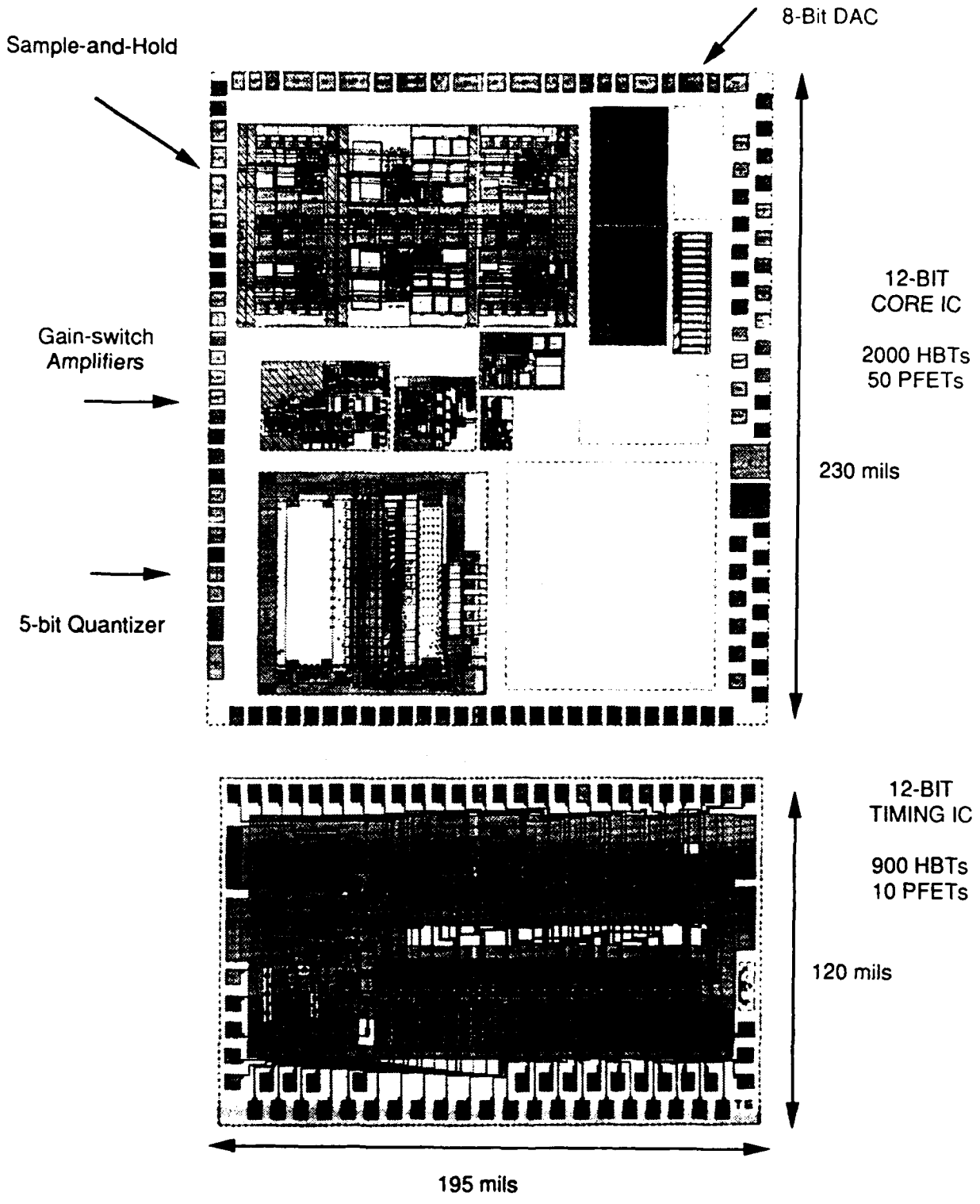

Figure 1. 12-bit ADC IC layout progress.

Layout of the 12-bit ADC core IC is approximately 75% complete, while layout of the timing and control IC is 100% complete. The S/H, 5-bit quantizer, gain switched residue amplifier, and timing and control circuitry are in final layout verification. Layout of the 8-bit digital-to-analog converter (DAC), error correction, and TTL output circuitry continues.

Presently, Hughes has inadequate funding to complete the 12-bit effort. Hughes and TI are negotiating a strategy for successful completion of the program. Assuming funding issues are resolved by 1 July, the 12-bit ADC will be released for fabrication by mid August.

C. New 5-Bit and 8-Bit ADC Contract

The TI/Hughes team has negotiated a contract with a classified government program to complete and enhance the 5-bit and 8-bit ADC work started under this DARPA program. The program entails a two-pass design cycle for the 8-bit ADC. In the first-pass design, S/H circuits would be added to both the 5-bit and 8-bit ADCs. In addition, output levels of both ADCs would be made ECL compatible. All designs in the first-pass design would be made with an improved 5 × 5 μm^2 emitter HBT. After completion of the first-pass design, fabrication, and characterization, a second-pass design of the 8-bit-only ADC would be made using a scaled HBT with 2 × 5 μm^2 emitters to improve dynamic range to 7-bits for a 500-MHz bandwidth signal.

D. Personnel Assignments

There have been no changes in personnel.

IV. PLANS FOR NEXT QUARTER

Hughes Plans:

- Complete layout of the 12-bit ADC.

TI Plans:

- CRL will continue interfacing with the pilot line to ensure smooth process transfer
- The pilot line will complete characterization of PJFET lot
- The pilot line will start processing the 12-bit ADC.

F.J. MORRIS, Principal Investigator
System Components Laboratory

H.T. YUAN, Manager
GaAs Logic and Memory Branch

W.R. WISSEMAN, Program Manager
System Components Laboratory